



Signal Integrity Measurement Analysis

Uncover delays, ringing, crosstalk, and EMI early
in a high-speed digital design

Signal integrity (SI) addresses two key aspects of high-speed digital design: signal timing and quality. SI analysis ensures that signals reach their destination in good condition. For example, a system with good signal integrity has data that arrives early enough to meet timing requirements and to avoid false clocking (where a clock crosses a logic threshold more than once during a transition).

In a system, signals travel through various kinds of interconnections. For example, from chip to package, package to board trace, and trace to high-speed connectors. Signal integrity problems arise from the physical nature of the interconnecting wires. Unlike a connection line drawn on a schematic, a real wire has resistance, capacitance to ground and to other wires, and inductance. At higher frequencies, capacitance and inductance cause the wire to act as a transmission line. The resulting antenna effects result in crosstalk and electromagnetic interference (EMI).

Sufficiently significant signal-integrity problems cause systems to fail or work only intermittently, producing “bad” data. It is crucial to find signal integrity problems early in a design cycle. Intermittent failures are difficult to debug on prototypes.

Highlights in this paper includes:

- High-speed digital design challenges
- Signal integrity analysis techniques
- Power of S-parameters

High-Speed Digital Design Challenges

New standards bring faster speeds and more test factors to consider. Today's radio frequency (RF) and microwave designs require multi-chip modules with more elaborate interconnects and packaging. The complexity continues to increase. 5G, for example, requires higher frequencies and broader modulation bandwidth. There are more simulation and measurement data to analyze than ever before. Despite these time-consuming challenges, designers need to accelerate their time to market to stay ahead of the competition.

Designs must meet electromagnetic interference and compliance regulations. Electromagnetic emissions from a device or system that interfere with the normal operation of another device or system are known as electromagnetic interference (EMI). A system's ability to operate without introducing an intolerable electromagnetic disturbance is known as electromagnetic compliance (EMC). Designers must also ensure their devices meet EMI and EMC regulations.

Performing signal integrity analysis with accuracy, in a reasonable amount of time, is a key challenge. Densely-routed boards require hours of engineering time to achieve accurate SI results — including many hours of simulation. Often, designers can only verify small sections of the board at one time. Hybrid simulation is much faster by comparison and provides greater coverage. The connectors and board integrate together and simulated using planar and 3D electromagnetic (EM) simulation. However, there is always the question of whether the simulation correlates well with the measurement. It is possible to miss some EM effects using the simplified techniques.

Memory designs continue to grow in complexity. Double data rate (DDR) memory designs become more complex with each new generation. Simulation and test configurations also increase in complexity, resulting in longer simulation and test setup times. This added complexity makes it challenging to correlate simulation and test data, resulting in less confidence in designs, longer troubleshooting cycles, and missed delivery schedules. Hardware designers working on memory systems must contend with both shrinking timing and voltage margins, and a complex list of compliance measurements to ensure reliable operation. As the industry moves to DDR4 and beyond, random jitter becomes much more significant. Designers need to ensure that their memory designs will pass receiver tests at ultra-low bit error rates (BERs).

The traditional approach to determine the root cause of degradation (for example, delays, ringing, crosstalk, and EMI) is to use analysis techniques like eye diagrams, single pulse response, time-domain reflectometry (TDR), and mixed-mode S-parameters.

With increasing data rates in computers, networks, storage, and mobile devices, design engineers need to address traditional emissions issues, as well as coupling issues with nearby circuit and system components.

Signal Integrity Analysis Techniques

The standard approach to examine any interconnect is the eye diagram. Eye diagrams give us a concise graphical representation of how the channel degrades the signal. An open eye corresponds to minimal signal distortion. It is easy to distinguish between a digital one and a zero level. However, loss and reflections in the system cause the eye to close, corresponding to distortion of the signal. It is then more difficult for the receiver to tell a digital one from a zero and indicates a signal integrity problem.

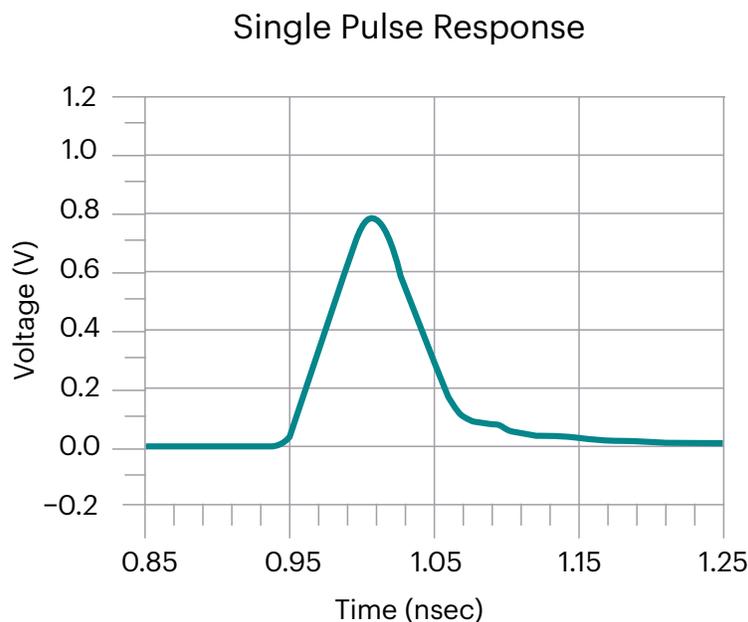


Figure 1. Single-pulse response sends data in one pulse and then examines how the channel affects the single pulse

In a single pulse response, a single pulse is sent with a specific rise time and data rate. You can examine how the channel affects the single pulse at the output. A single pulse response takes complex data in one pulse, reducing complexity, and then examines how the channel affects the single pulse. The definition of bit rate is the rise time of the pulse and the width.

Developing a controlled impedance environment for high-speed digital signals is the best way to guarantee a clean data transmission channel with no bit errors at the receiver. In applications involving signals with rise times shorter than one nanosecond, transmission line properties of the interconnects become critical. In time-domain reflectometer (TDR) measurements, a fast-rising step edge is sent into the device under test to measure the reflected signal. TDR measurements help to avoid issues like crosstalk, impedance mismatch, reflections, amplitude degradation, and skew.

Measurements in the time and frequency domains are related. A typical measurement in the time domain is a TDR measurement, which is the measure of the signals reflected from the device's input as a function of time. These are known as T-parameters. The equivalent in the frequency domain is the S-parameter, which is the ratio of the reflected wave to the incident wave.

The Power of S-Parameters

S-parameters are the shared language between simulation and measurement. They are a matrix that shows reflection/transmission characteristics (amplitude/phase) in the frequency domain. S-parameter measurements are critical in high-speed digital applications and have increased in importance due to the emergence of gigabit channels in data networks.

S-parameters are the de facto standard for engineers to describe the frequency behavior of a given device. Time-domain reflectometry provides spatial and timing information. Frequency response S-parameters transform into time domain parameters by performing an inverse Fast Fourier transform (IFFT). The S-parameters of an interconnect, whether measured in the time or the frequency domain, represent a behavioral model of the interconnect. They contain all the information about how a signal entering one port will behave when it exits another port.

A two-port device has four S-parameters. The numbering convention for S-parameters is the first number following the "S" is the port where the signal emerges. The second number is the port where the signal is applied. S₂₁ is a measure of the signal coming out port two relative to the stimulus entering port one. When the numbers are the same (for example, S₁₁), it indicates a reflection measurement. In this case, the input and output ports are the same.

The information provided by four-port differential S-parameters is the principal means to describe the electrical properties of any four-port interconnect. In the complete matrix of measured four-port S-parameters, there is an abundance of data. There are 16 possible combinations of waves going in and out. The 16 differential S-parameter matrix elements contain everything you need to know about the electrical properties of a differential pair.

In cases where more detailed information is necessary, you can use the exported S-parameters as a behavioral model and integrate them directly into circuit simulators in electronic-design automation tools.

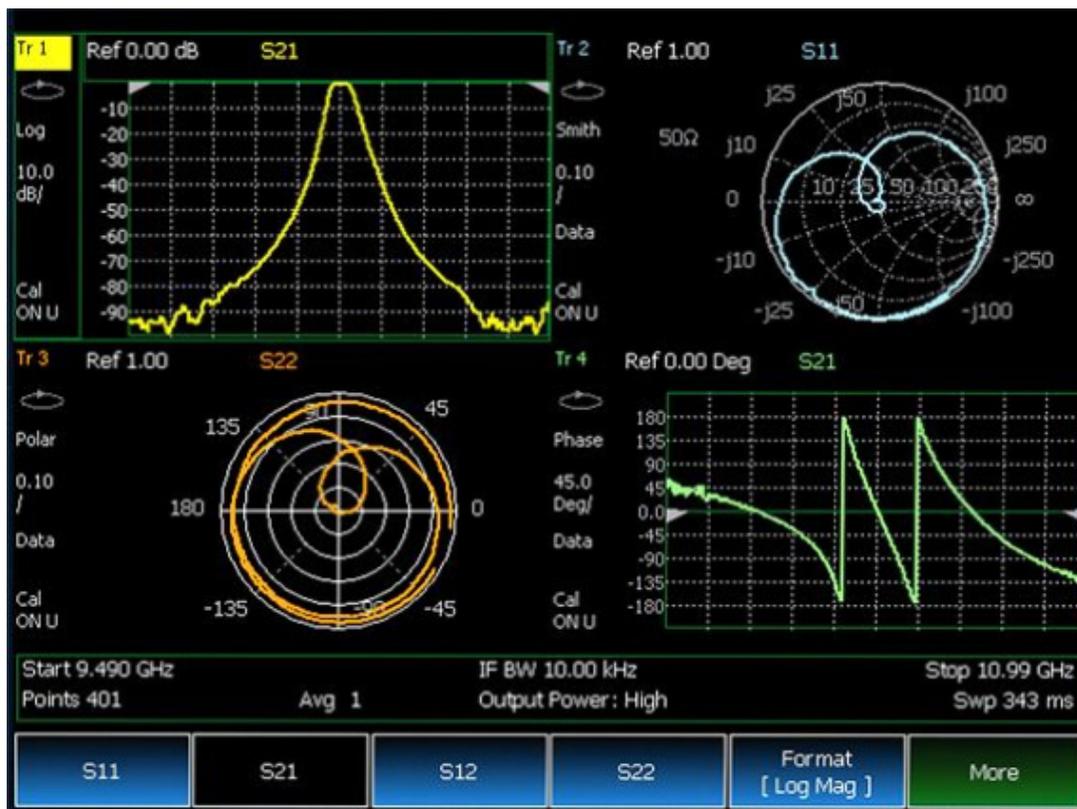


Figure 2. S-parameters allow engineers to gain valuable insight into the performance of high-speed digital interconnects like backplanes, printed circuit boards, cables, connectors, and even IC packages

Conclusion

For today's high-speed boards and integrated circuits, SI is as important to specify as digital functionality or clock speed. Addressing signal integrity issues in densely packed, low power, small form factor circuits is challenging. It is often difficult for designers to know when signal integrity issues exist and how to find them.

The following three steps help to solve signal integrity problems:

- simulate the channel
- identify the root cause of degradation
- explore design solutions

A variety of signal integrity analysis methods help resolve signal degradation difficulties, including eye diagrams, single pulse response techniques, mixed-mode S-parameters, and time-domain reflectometry. As part of a good design practice, and to ensure the quality of signal transmissions, engineers should consider signal integrity from the time they draw the schematic until the board passes its final test. By addressing signal integrity problems early, you ensure optimal circuit design and development that works reliably at a reasonable cost.

Related Links

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